Examiner Amendment

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Cory G. Claassen on 6/17/10.

Claims

Claim 4 (Currently Amended): The apparatus of claim 3, wherein the input processing element generates the initial bit reliability as equaling an absolute value of a value corresponding to the bit positions, and the initial hard decision value as equaling a second value if the soft decision value is positive and a third value otherwise.

Claim 9 (Currently Amended): The apparatus of claim 8, wherein the first set of associative processing elements comprise a first element, which further comprises a logic inside the processing logic unit to receive the one or more control values and generate update values, wherein the update values, wherein the update values represent a result of comparison of masked on bits of the first comparand and the bit reliability value stored in the first

element, and a set of logic gates inside the processing logic unit to generate the one or more decision values based on the update values and send the decision values to a second element.

Claim 25 (Currently Amended): The system of claim 21, wherein the system further includes at least one of a computer, a switch, a router, a handheld, a cell phone, or a server.

Claim 16 (Currently Amended) A method comprising: ~~determining a first minimum value and a second minimum value of bit reliability values stored in a first set of associative processing elements during a first iteration.~~

operating a plurality of processing elements based on associative processing, the plurality of processing elements performing operations in word-parallel, bit-serial format; and

iteratively decoding, with the plurality of processing elements, a received codeword using a bit reliability value such that for each iteration, the bit reliability value is updated based on a comparison using a threshold value based on a plurality of threshold values that are updated during the iterative decoding,

wherein each processing element in the plurality of processing elements includes:

a memory unit for storing data, wherein the data stored within the memory unit is identified based on memory content rather than an address; and

a processing logic unit for comparing the bit reliability value with the threshold value.

Claim 17 (Currently Amended) The method of claim 16 further comprising: ~~comprises~~

determining a first minimum value and a second minimum value of bit reliability values stored in a first set of associative processing elements during a first iteration;

storing the first minimum value in the first set of associative processing element comprising a value other than the first minimum value[[,]]; and

storing the second minimum value in the first set of associative processing elements that stored the first minimum value before the first iteration.

Claim 18 (Currently Amended) The method of claim [[16]]17 further comprising: ~~comprises~~

generating one or more control values comprising a first comparand and a mask to determine the presence of the first minimum value in the first set of associative processing element[[,]];

generating a second comparand and a mask to determine the presence of the second minimum value in the first set of associative processing element,

receiving one or more decision values indicating presence of one or more of the first minimum value and the second minimum value[[,]]; and

determining the first minimum value and the second minimum value based on the one or more decision values.

Claim 19 (Currently Amended) The method of claim 18 further comprising: ~~comprises~~

receiving the one or more control values[[,]];

generating the one or more decision values comprising a first value indicating a presence of the first minimum value in at least one of the first associative processing elements[[,]];

generating the one or more decision values comprising a second value indicating a presence of the second minimum value in at least one of the first associative processing elements[[,]]; and

generating the one or more decision values comprising a third value indicating a presence of the first minimum value in at least two of the first associative processing elements.

Claim 20 (Currently Amended) The method of claim 19 further comprising: ~~comprises~~

receiving the one or more control values[[,]];

generating a first update value, wherein the first update value represents a result of comparison of masked-in bits of the first comparand and a first bit reliability value[[,]]; and

generating a second update value, wherein the second update value represents a result of comparison of masked-in bits of the second comparand and a first bit reliability value.

Reasons for Allowance

Claims 1-26 are allowable over the prior art.

The following is an Examiner's statement of reasons for allowance: the prior art fails to teach features of the claimed invention.

It has been determined after careful review of the claims, when read as a whole, that the prior art does not teach: a plurality of processing elements operating based on associative processing, the plurality of processing elements coupled to perform operations in word-parallel, bit- serial format, wherein the plurality of processing elements are further coupled to iteratively decode a received codeword using a bit reliability value such that for each iteration, the bit reliability value is updated based on a comparison using a threshold value based on a plurality of threshold values that are updated during the iterative decoding, each processing element in the plurality of processing elements further including: a memory unit for storing data, wherein the data stored within the memory unit is identified based on memory content rather than an address.

Conclusion

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Enam Ahmed whose telephone number is 571-270-1729. The examiner can normally be reached on Mon-Fri from 8:30 A.M. to 5:30 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman, can be reached on 571-272-3644.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EA

6/8/10

/Scott T Baderman/

Supervisory Patent Examiner, Art Unit 2114